Do current sources perform to "spec," as simulated? Hardware for evaluating simulator accuracy

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Abstract: Ultimately, we aim to test the performance of current sources in SPICE simulation and on biological loads by building representative hardware. We present a preliminary hardware design in this paper.

1 Introduction

In this work, we describe our hardware under development (Figure 1), the drive portion of an EIT system, which implements a variety of current source topologies. We aim to use this hardware to take lab measurements and characterize deviations from expected (SPICE simulated) results on resistor or resistor-capacitor (R/RC) phantoms, biological models, and human volunteers. In the following, we describe the preliminary hardware design.

2 Back end: digital control and synthesis

The back end of the hardware design consists of a microcontroller (STM32F205, ARM Cortex-M3, STMicroelectronics) supporting USB 2.0 and microSD storage. Power is supplied via USB port and a lithium ion battery. An FPGA (XC6SLX9, Spartan6, Xilinx) provides direct digital synthesis (DDS) connected to a 16-bit digital to analog convertor (DAC) (AD5542A, Analog Devices). An integrated DDS/DAC (AD9837, Analog Devices) is also supported. Sync and trigger connectors (SMA) wired to the FPGA support external test and measurement infrastructure.

3 Front end: current sources, switching, isolation

The preliminary design supports current source topologies often selected for EIT designs. These topologies include Howland [1], enhanced Howland [2–5], modified enhanced Howland [6], bipolarity source-sink [1], current conveyor II (CCII) / current feedback opamp [4, 7], and cascode current sources [1]. Except for the last two sources, these current sources are all closely related designs. A repeated common layout is supported for the majority of the current sources so that a variety of designs can be explored with minimal board rework.

To model instrument loads, a transformer-based isolation strategy is implemented at the current source. Beyond the isolation, a switch network models capacitive loads for (effectively) an 8 to 256 electrode array. At the board output, off-board connectors (SMA) enable wiring harness and electrode connections to alternative phantoms and human volunteers.

4 Simulated Performance

Performance of an enhanced Howland current source was simulated in Figure 2 (a) transient simulation, and (b) frequency response for an LM741-based design (Texas Instruments) when resistors exhibit a 10% mismatch.

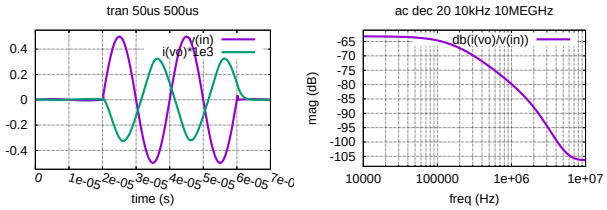

Figure 2: Howland current source (left) transient (50 kHz input), and (right) current gain versus frequency simulated in `ngspice-30` using an LM741 SPICE model (Texas Instruments)

5 Conclusions

This work illustrates preliminary work on hardware to be used in validating SPICE simulations of a variety of current source topologies. It is hypothesized that simulations will *not* correlate for biological media due to Cole-Cole type dispersions.

We welcome input on your personal experiences designing EIT hardware and any comments or suggestions you have on our own hardware design.

References

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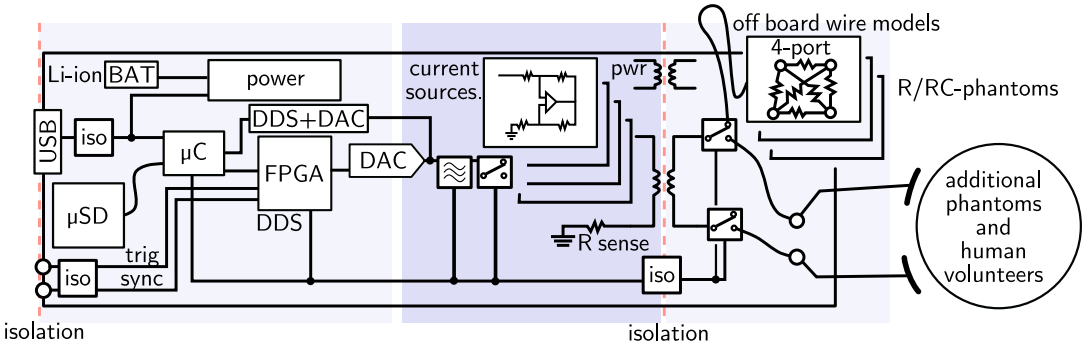

Figure 1: Block diagram showing the structure of the EIT current source test fixture